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06/848,017	04/03/1986	GILBERT P. HYATT	307	7574

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2189	

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DATE MAILED: 03/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

REQUIREMENT FOR INFORMATION UNDER 37 C.F.R. § 1.105

1.   Applicant and the assignee of this application are required under 37 CFR 1.105 to

provide the following information that the examiner has determined is reasonably necessary to

the examination of this application. See *Star Fruits S.N.C. v. United States*, 73 USPQ2d 1409

(CA FC 2005).

Stipulations

2.   In response to this requirement, please agree or disagree to the stipulation of each of the

following assertions of facts:

1. Attached "Exhibit A" is a correct representation of Applicant's claim for priority under

    35 U.S.C. §120 based on Applicant's statements on pages 37-40 of the amendment

    received 30 July 1990.

2. The terminology "alterable memory" (e.g. claim 102), "random access memory" (e.g.

    claim 5), and "operand memory" (e.g. claim 104) as used throughout the claims refers to

    the same memory and are in fact just different labels with no patentable distinctions and

    therefor are equivalent structures.

3. The terminology "integrated circuit digital signal processor" (e.g. claim 42), "single

    integrated circuit chip having a digital signal processor" (e.g. claim 53), and "monolithic

    integrated circuit data processor" (e.g. claim 164) as used throughout the claims refers to

    the same "single-chip" processor and are in fact just different labels with no patentable

    distinctions and therefor are equivalent structures.

For the first stipulation Applicant is required to review Exhibit A and state whether Applicant

agrees or disagrees with how applicant's claims for priority are portrayed in the priority tree. If

Applicant disagrees with the portrayal of applicant's claims for priority in the priority tree

(shown as Exhibit A), then Applicant must specifically point out the changes necessary, and how

the statements on pages 37-40 of the 30 July 1990 amendment support these changes.

With regard to the second and third stipulations, it is reasonably necessary to the examination

of the application to ascertain whether there are any differences of any significance among these

terms and how such differences are to be attributed. Applicant is required to point out the

differences between the terms (if any) and how these differences are supported in the

specification, or the prior art at the time the invention was made.

Interrogatories

3.   In response to this requirement, please provide answers to each of the interrogatories

eliciting factual information set forth below. In order to properly consider prior art references, it

is reasonably necessary to the examination for the examiner to know which applications among

those claimed for priority support the following claim limitations and the phrasing used in the

earlier applications. The phrasing and scope of the earlier filed applications are particularly

relevant to the examiner's development of search terms and methodology, because of the

changes in vernacular within the subject matter technology over the time horizon embodied

within the applicant's priority claims.

It is also relevant to properly construing the scope of the claimed subject matter relative

to the disclosure, and whether there are any differences in the implied scope relative to the

teachings in each of the priorities claimed. The applicant, having prepared the applications, is in

a far superior position than the examiner to show the correlation so needed, and the nesting of the

claims for priority are particularly complex, and therefore it is reasonable to require this

necessary information from the applicant for the reasons of both increased efficiency and

accuracy in the overall prosecution.

Applicant is required to show how each of the following claim limitations are supported in

the parent applications in accordance with the written description and enablement requirements

of 35 U.S.C. §112, first paragraph as well as the requirements of 37 CFR 1.75(d)(1). Applicant

should reference each parent application that supports a particular limitation, and for each

parent application referenced, indicate the specific page and line numbers and/or figure(s) (with

reference to specific elements within the figure(s)) that provide support for the limitation.

1. "generating pattern recognition information in response to the digital signal processor

   program, in response to the digital signal processor operands, and in response to the input

   information" (e.g. claim 46).

2. "an amplifier coupled to the antenna and generating amplified information in response to

   the antenna information" (e.g. claim 47)

3. "generating data compressed information with an integrated circuit digital signal

   processor in response to the digital signal processor program, in response to the digital

   signal processor operands, and in response to the input information." (e.g. claim 48).

4. "generating iteratively processed information in response to the digital signal processor

   program, in response to the digital signal processor operands, and in response to the input

   information" (e.g. claim 57).

5. "filter processor" (e.g. claim 59).

6. "correlator filter processor" (e.g. claim 60).

7. "an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating correlation product operands by multiplying operands in response to the instructions and an integrated circuit adder circuit coupled to the integrated circuit read only memory and to the integrated circuit multiplier circuit and generating correlation filtered operands by adding the product operands in response to the instructions" (e.g. claim 60).

8. "generating searched information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information" (e.g. claim 61).

9. "generating matched information with an integrated circuit digital signal processor in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information" (e.g. claim 63).

10. "an integrated circuit synchronization circuit generating a synchronization information" (e.g. claim 67).

11. "an integrated circuit multiple loop iterative processing circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and iteratively generating filtered operands" (e.g. claim 69).

12. "a refresh circuit coupled to the integrated circuit dynamic random access alterable memory and refreshing the integrated circuit dynamic random access alterable memory" (e.g. claim 76).

13. " a loop heading circuit", "a loop initializing circuit", "a loop looping circuit", "a skipping circuit", "a loop update circuit", "a first output circuit generating product information in response to the input information and in response to the updated loop information", "a second output circuit generating output rounded off product information in response to the product information" and "a loop exiting circuit" (e.g. claim 99).

14. "an outer loop header circuit", "an outer loop initializing circuit", "an outer loop looping circuit", "an outer loop update circuit", "a middle loop header circuit", "a middle loop initializing circuit", "a middle loop looping circuit", "a middle loop update circuit", "an inner loop header circuit", "an inner loop initializing circuit", "an inner loop looping circuit", "a skipping circuit", "an inner loop update circuit", "a first output circuit generating updated inner loop information in response to the looping through the inner loop", and "a second output circuit generating output rounded off change information in response to the change information" (e.g. claim 104).

15. "generating radar image information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information" (e.g. claim 107).

16. "generating medical information with an integrated circuit digital signal processor in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information" (e.g. claim 108).

17. "an integrated circuit interrupt execution circuit coupled to the integrated circuit instruction execution circuit and coupled to the integrated circuit interrupt input circuit, the integrated circuit interrupt execution circuit interrupting the generating of the first

processed information by the integrated circuit instruction execution circuit in response to

the input interrupt information generated by the integrated circuit interrupt input circuit"

(e.g. claim 109).

18. "generating seismic information in response to the digital signal processor program, in

response to the digital signal processor operands, and in response to the input

information" (e.g. claim 112).

19. "an integrated circuit indexing circuit coupled to the integrated circuit read only memory

address circuit and coupled to the integrated circuit index memory, the integrated circuit

indexing circuit generating an indexed instruction address in response to the index

operand stored in the index memory and in response to at least one of the instruction

addresses generated by the integrated circuit read only memory address circuit" (e.g.

claim 115).

20. "the integrated circuit read only memory accessing circuit further coupled to the

integrated circuit indirect transfer memory and generating an accessed indirectly

transferred computer instruction in response to at least one of the computer instructions

stored in the integrated circuit read only memory, in response to the indirect transfer

address stored in the integrated circuit indirect transfer memory, and in response to the

indirect transfer information generated by the integrated circuit indirect transfer circuit"

(e.g. claim 115).

21. "an integrated circuit read only memory accessing circuit generating an accessed directly

transferred computer instruction in response to at least one of the computer instructions

stored in the integrated circuit read only memory and in response to the direct transfer
information generated by the integrated circuit direct transfer circuit" (e.g. claim 119).

22. "generating processed information with an integrated circuit digital signal processor
having an indirect transfer instruction" (e.g. claim 122).

23. "generating processed information with an integrated circuit digital signal processor
having an index instruction" (e.g. claim 124).

24. "A digital signal processor comprising:…an integrated circuit interrupt execution
circuit…an integrated circuit indexing circuit…an integrated circuit direct transfer
circuit…an integrated circuit indirect transfer circuit…an integrated circuit instruction
execution circuit" (e.g. claim 125).

25. "a frame loop header circuit", "a frame loop initializing circuit", "a frame loop looping
circuit", "a frame loop update circuit", "a block loop header circuit", "a block loop
initializing circuit", "a block loop looping circuit", "a block loop update circuit", "a
sample loop header circuit", "a sample loop initializing circuit", "a sample loop looping
circuit", "a skipping circuit", "a sample loop update circuit", "a first output circuit
generating product information in response to the input information and in response to
the updated sample loop information", and "a second output circuit generating output
rounded off product information in response to the product information" (e.g. claim 134).

26. "a communication circuit coupled to the integrated circuit instruction execution circuit
and communicating information to a remote location in response to the processed
information generated by the integrated circuit instruction execution unit" (e.g. claim
136).

27. "generating processed information with an integrated circuit digital signal processor having a read only memory write instruction" (e.g. claim 140).

28. "generating processed information with an integrated circuit digital signal processor having a decrement instruction" (e.g. claim 142).

29. "generating processed information with an integrated circuit digital signal processor having a decrement and transfer instruction" (e.g. claim 144).

30. "generating processed information with an integrated circuit digital signal processor having a conditional transfer instruction" (e.g. claim 146).

31. "generating processed information with an integrated circuit digital signal processor having a skip on condition instruction" (e.g. claim 156).

32. "generating processed information with an integrated circuit digital signal processor having a serial input instruction" (e.g. claim 157).

33. "generating processed information with an integrated circuit digital signal processor having a serial output instruction" (e.g. claim 158).

34. "generating processed information with an integrated circuit digital signal processor having a discrete output instruction" (e.g. claim 159).

35. "generating processed information with an integrated circuit digital signal processor having a skip on discrete instruction" (e.g. claim 166).

36. "generating processed information with an integrated circuit digital signal processor having power turn on interrupt instruction" (e.g. claim 168).

37. "a machine data processor implemented on a single integrated circuit chip" (e.g. claim 171).

38. "a data processor implemented on a single integrated circuit chip" (e.g. claim 172).

39. "a photo optical machine coupled to the data processor implemented on the single integrated circuit chip, the photo optical machine generating a photo optical mask in response to data processed by the data processor" (e.g. claim 174).

40. "a pattern generator coupled to the data processor implemented on the single integrated circuit chip, the pattern generator machine generating a pattern in response to data processed by the data processor" (e.g. claim 175).

41. "a plotter coupled to the data processor implemented on the single integrated circuit chip, the plotter generating a plot in response to data processed by the data processor" (e.g. claim 176).

42. "a read only memory implemented on a single integrated circuit chip; and an alterable memory implemented on the single integrated circuit chip" (e.g. claim 177).

43. "generating processed information with an integrated circuit digital signal processor having save return address microinstruction in response to the digital signal processor program and in response to the input information" (e.g. claim 184).

44. "making a disk memory product in response to the processed information" (e.g. claim 188).

45. "writing digital signal processor operands into the integrated circuit read only memory in response to the digital signal processor program and in response to the input information" (e.g. claim 202).

46. "making a payroll product in response to the first processed information" (e.g. claim 212).

47. "making an inventoried product in response to the second processed information" (e.g. claim 218).

48. "making a natural resource product in response to the first processed information" (e.g. claim 225).

49. "making a telephone product in response to the first processed information" (e.g. claim 226).

50. "making a mineral product in response to the third processed information" (e.g. claim 234).

51. "making a moving product in response to the first processed information" (e.g. claim 241).

52. "making an oil product in response to the first processed information" (e.g. claim 246).

53. "making a turret product in response to the first processed information" (e.g. claim 248).

54. "making a vehicle product in response to the fourth processed information" (e.g. claim 294).

Conclusion

4.   The fee and certification requirements of 37 CFR 1.97 are waived for those documents submitted in reply to this requirement. This waiver extends only to those documents within the scope of this requirement under 37 CFR 1.105 that are included in the applicant's first complete communication responding to this requirement. Any supplemental replies subsequent to the first communication responding to this requirement and any information disclosures beyond the scope of this requirement under 37 CFR 1.105 are subject to the fee and certification requirements of 37 CFR 1.97.

5.   The applicant is reminded that the reply to this requirement must be made with candor and good faith under 37 CFR 1.56. Where the applicant does not have or cannot readily obtain an item of required information, a statement that the item is unknown or cannot be readily obtained may be accepted as a complete reply to the requirement for that item.

6.   This requirement is subject to the provisions of 37 CFR 1.134, 1.135 and 1.136 and has a shortened statutory period of 2 months. EXTENSIONS OF THIS TIME PERIOD MAY BE GRANTED UNDER 37 CFR 1.136(a).

7.   Any inquiry concerning this communication should be directed to Reginald G. Bragdon whose telephone number is (571) 272-4204. Mr. Bragdon can normally be reached on Monday-Thursday from 5:30 AM to 2:30 PM and every other Friday from 5:30 AM to 2:30 PM.

Reginald G. Bragdon
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RGB   Supervisory Patent Examiner
March 16, 2006   Art Unit 2189